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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,406	10/29/2003	Russell W. Guenthner	52003218	7204

7590 06/06/2006

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,406	GUENTHNER ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/697,406 and RCE with amendment filed on 4/12/2006. Claims 1-6 remain pending in the application.

Claim Objections

2. Claim 1 is objected to because of the following informalities: step b) "analyzing the timing paths" should be changed to –analyzing timing paths--; step e) "implementing in another way the critical logic" should be changed to –implementing a new way a critical logic--; "the chosen critical path" should be changed to –a chosen critical path--; "a duplication of the logic elements" should be changed to –a duplication of logic elements--. Claim 2, line 2, "in a new way" should be changed to --in said new way--. Claim 3, step a) and step b) should be changed to --step f) and step g) respectively; "step e) of claim 1" should be changed to --step e)-- in second occurrence. Claim 4, line 2, "in a new way" should be changed to --in said new way--. Claim 5, step b) "a plurality of elements" should be changed to –a plurality of logic elements--; step e) "the elements" should be changed to --said logic elements--. The proposed changes correct minor informalities to provide proper claim antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Beraudo et al., "Timing Optimization of FPGA Placement by Logic Replication," ACM 2003, June 3-6, 2003, pages 196-201.

5. As to claim 1, Beraudo et al. teach substantially the same claim invention of timing optimization of FPGA placement by logic replication (logic duplication) (see entire document). Fig. 2 shows synthesizing an overall logic for a first implementation in the FPGA including construction and a first placement of one or more logic functions on the FPGA, timing paths are analyzed and one or more critical timing paths are identified; a logic element (logic element C) on the critical paths are is selected for duplication. Fig. 3 shows implementing a new placement (in a new way or in another way of implementation of placement) by duplicating logic element(s) (replication of logic elements) utilized in the first placement (Fig. 2). The duplicated logic C' in the new placement provide an interconnect routing that is used to minimize interconnect routing distance of a chosen critical path than the first placement. Figs. 2-3 show interconnect routing of critical paths from a source to sink(s) (loads) with relative disregard as to the fanout of signals to other loads. Note that Figs. 2-3 are illustrated as examples. For example, interconnect routing from source D to loads A and E. In FPGA, complex circuits having different configuration of source and sinks interconnect routing are known and recognized by practitioners in the art.

6. As to claim 5, remarks set forth in rejecting claim 1 equally apply in rejection of claim 5 because of the same claim invention.

7. As to claim 2, Beraudo et al. teach that the limited implementation of placement Fig. 3 (a new placement) from Fig. 2 placement is only by duplicating logic element(s) on selected critical paths to provide new placement and routing structure to minimize interconnect routing.

8. As to claim 3, Fig. 3 shows example of timing optimization of FPGA placements by logic replication (logic duplication or modifying placement by logic duplication to minimize interconnect routing of selected critical path). In order to complete timing optimization of FPGA placements by logic replication on a plurality of critical timing paths as taught by Beraudo, this process is repeated (modifying second placement by repeating the same process which is timing optimization of FPGA placements by logic replication) to minimize interconnect routing for all said critical timing paths. Since other critical timing paths can be identified after last implementation, the repeat process of timing optimization must be repeated using this last implementation as basis for starting the timing optimization as taught by Beraudo in order to result said identified timing critical paths to thereby provide an overall circuit design with optimal timing paths. Thus this repeat process must use last implementation as basis for further perform timing optimization using the concept of timing optimization as taught by Beraudo to result any timing critical path that may be identified after last implementation.

9. As to claim 4, Beraudo et al. teach that the limited implementation of placement Fig. 3 (a new placement) from Fig. 2 placement is only by duplicating logic element(s)

on selected critical paths to provide new placement and routing structure to minimize interconnect routing.

10. As to claim 6, remarks for in rejection claim 3 equally apply. In addition, Fig. 3 shows example of timing optimization of FPGA placements by logic replication (logic duplication or modifying placement by logic duplication to minimize interconnect routing of selected critical path). This process is repeated to minimize interconnect routing for all critical timing paths by the timing optimization of FPGA placements by logic replication. The repeat process provides an overall circuit design with optimal timing paths.

Remarks

11. This new ground of rejection is based on the amendment filed with RCE on 4/12/06.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER